L Number	Hits	Search Text	DB	Time stamp
3	2571	segment$3 near3 (bus or busses or buses)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
4	201	(repeat$3 or retransmi$6) same (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:11
5	35	710/$.ccls. and ((repeat$3 or retransmi$6) same (segment$3 near3 (bus or busses or buses)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:10
6	0	('not' near3 (repeat$3 or retransmi$6)) same (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
7	0	('not' near5 (repeat$3 or retransmi$6)) same (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
8	0	("not" near5 (repeat$3 or retransmi$6)) same (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
9	0	("not" near5 (repeat$3 or retransmi$6)) and (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
10	0	(segment$3 near5 (bus or busses or buses)) and ("not" near5 (repeat$3 or retransmi$6))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:20
11	0	(segment$3) same ("not" near5 (repeat$3 or retransmi$6))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:21
12	0	(segment$3) same ("not" near10 (repeat$3 or retransmi$6))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:21

09/846,960

US-PAT-NO: 5528765

DOCUMENT-IDENTIFIER: US 5528765 A
See image for Certificate of Correction

TITLE: SCSI bus extension system for controlling individual arbitration on interlinked SCSI bus segments

DATE-ISSUED: June 18, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Milligan; James H.	Shoreview	MN	N/A	N/A

US-CL-CURRENT: **710/107**, 370/451 , 370/462 , 709/225 , 709/249

ABSTRACT:

This digital communication method and system permits extended distance communication on a SCSI bus despite the time constraints imposed on certain bus operations such as arbitration. The bus system is comprised of discrete bus segments each having a portal node and one or more devices interfaced thereon. All nodes are connected together by a serial link. Each node seizes control of its bus segment and imposes a pseudo-busy condition to prevent bus operations such as arbitration. A token message passed over the serial link between nodes allows one node at a time to release control of its segment to permit arbitration among the devices interfaced on its segment. A source device on the released segment that gains control of the segment as a result of arbitration may communicate with a destination device anywhere on the bus system.

37 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

---------- KWIC ---------

Detailed Description Text - DETX (10):

Serial messages illustratively travel in one direction (e.g., clockwise or counterclockwise) for a ring configuration. For example, a message at the terminating end of link portion 14 is sampled, or "read" or detected, by the internal circuitry of node 20 for possible transfer to its **bus segment**. Where appropriate, the message is **retransmitted** onto the originating end of link portion 16 to downstream node 22. In the case of a token message, the return of the token back to the node that created it (e.g., the primary node such as node 20) will be recognized by that node when it examines the message (and the primary node may or may not end up **retransmitting** the token message).

Current US Original Classification - CCOR (1):

710/107

US-PAT-NO: 6591322

DOCUMENT-IDENTIFIER: US 6591322 B1

TITLE: Method and apparatus for connecting single master devices to a multimaster wired-and bus environment

DATE-ISSUED: July 8, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ervin; Joseph J.	Stow	MA	N/A	N/A
Lach; Jorge E.	Lexington	MA	N/A	N/A

US-CL-CURRENT: **710/110**, **710/314** , 711/201

ABSTRACT:

A "firewall" apparatus is placed between a single bus master device and a multimaster I.sup.2 C bus system. The firewall apparatus transforms all multimaster bus errors into simple NAK errors and isolates the single bus master from the multimaster bus. Therefore the single bus master needs only to retry transactions that receive unexpected NAKs and all complex multimaster issues, such as bus collisions, transaction termination and bus recovery, associated with the actual error that occurred on the multimaster bus are handled by the firewall apparatus. In accordance with one embodiment, when the single bus master attempts to launch a transaction at a time when the multimaster I.sup.2 C bus is busy, the firewall apparatus absorbs the address driven by the single bus master and then stalls the transaction until the firewall apparatus is able to successfully acquire and drive the address on the multimaster bus. The firewall apparatus is implemented in a preferred embodiment by a programmed microcontroller.

26 Claims, 16 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 15

---------- KWIC ---------

Detailed Description Text - DETX (2):

The invention concerns a "firewall" apparatus and method that buffers I.sup.2 C transactions generated by a bus master and **retransmits** the transactions on a multimaster **bus segment**. The term "firewall" refers to the fact that the inventive apparatus is an asymmetric bus bridge. Thus, it operates in a fashion similar to an Internet firewall that allows transparent access from a corporate intranet to the external Internet, while blocking Internet traffic from entering the corporate intranet. Similarly, the inventive apparatus possesses two I.sup.2 C ports, hereafter called "port-A" and "port-B", and functions to pass I.sup.2 C traffic transparently from port-A to port-B, but not vice versa. The term "port-A master" is used to refer to the master device connect to port-A on the private I.sup.2 C segment.

Detailed Description Text - DETX (83):

FIG. 12 shows the operation of the firewall apparatus during a **repeated** start condition driven by the port-A master 302. In this example, a transaction driven by the port-A master 302 is already in progress and is being passed to the multimaster I.sup.2 C **bus segment** 314. At the left of this figure, the port-A master 302 drives a **repeated** START condition to issue a new address during the current transfer. The firewall apparatus detects this **repeated** START and passes control to the flow shown in FIG. 7. It can be seen in the flow of FIG. 7 that the address bits following this **repeated** START condition are passed from port-A 308 to port-B 314 on a bit-by-bit basis. Thus, the latency added to the transaction by the firewall apparatus appears as a stretching of the LOW portions of the port-A and port-B SCL lines, 306 and 312. It is during these LOW times on the SCL lines 306, 312 that the firewall is servicing the other port.

Current US Original Classification - CCOR (1):
710/110

Current US Cross Reference Classification - CCXR (1):
710/314

PGPUB-DOCUMENT-NUMBER: 20020166011

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020166011 A1

TITLE: Method and apparatus for driving signals on a bus

PUBLICATION-DATE: November 7, 2002

INVENTOR-INFORMATION:

NAME RULE-47	CITY	STATE	COUNTRY
Bassett, David	San Jose	CA	US
Browning, Gary	Boulder Creek	CA	US

US-CL-CURRENT: **710/100**

ABSTRACT:

A method is provided for controllably delivering signals on a bus, wherein the bus is comprised of a first and second segment. The method comprises monitoring the first **bus segment** for the presence of a first signal being driven thereon. Thereafter, the first signal is **repeated** on the second **bus segment**. To prevent the **repeated** signal from being **repeated** again, the second **bus segment** is not monitored during the **repeating** phase of the operation.

---------- KWIC ---------

Abstract Paragraph - ABTX (1):

A method is provided for controllably delivering signals on a bus, wherein the bus is comprised of a first and second segment. The method comprises monitoring the first **bus segment** for the presence of a first signal being driven thereon. Thereafter, the first signal is **repeated** on the second **bus segment**. To prevent the **repeated** signal from being **repeated** again, the second **bus segment** is not monitored during the **repeating** phase of the operation.

Current US Classification, US Primary Class/Subclass - CCPR (1):

710/100

Summary of Invention Paragraph - BSTX (3):

[0002] This invention relates generally to driving signals on a bus, and, more particularly, to a **repeater** capable of driving a signal onto a plurality of **bus segments** with only a single clock delay.

Summary of Invention Paragraph - BSTX (9):

[0007] In one aspect of the present invention, a method is provided for controllably delivering signals on a bus wherein the bus is comprised of a first and second segment. The method comprises: monitoring the first **bus segment** for the presence of a first signal being driven thereon; **repeating** the first signal on the second **bus segment**; and preventing the first signal from being **repeated** on the first bus.

Detail Description Paragraph - DETX (11):

[0023] Turning now to FIG. 3, one embodiment of a portion of the **repeater** 210 is shown in functional block diagram form. In the illustrated embodiment, the **repeater** 210 is configured to monitor four **bus segments** for the presence of a signal on one of the segments, and then upon detecting such a signal, **repeating** the detected signal onto the remaining three **bus segments**. Each line in each of the four **bus segments** has a substantially identical driver associated with it in the **repeater** 210. Accordingly, for ease of illustration, only the drivers associated with all four **bus segments** of a single bit line is illustrated in FIG. 3. Those skilled in the art will appreciate that the circuitry shown herein may be **repeated** according the size of the bus. For example, if the bus is selected to be 170-bits wide, then the circuitry illustrated herein may be **repeated** 170 times so that all 170 bits on each **bus segment** may be monitored and **repeated onto the other bus segments**. Additionally, while the **repeater** 210 is illustrated as having four **bus segments,** more or fewer segments may be provided without departing from the scope of the instant invention.

Detail Description Paragraph - DETX (12):

[0024] As shown in FIG. 3, four bit lines 300A-300D are shown, where each of the four bit lines is associated with four segments 302A-302D, respectively. Four devices, such as microprocessors, may be coupled to each of the **bus segments**. Generally, the **repeater** 210 responds to a signal driven onto the bit line 300A of the **bus segment** 302A by **repeating** or driving the same signal onto the remaining bit lines 300B-300D of the **bus segments** 302B-302D.

Detail Description Paragraph - DETX (16):

[0028] Turning now to FIG. 4, one embodiment of a portion of the **repeater** 210 of FIG. 3 is shown in schematic form. The illustrated circuitry is comprised of four circuits 400A-400D. The receivers 304A-304D are respectively comprised of a comparator 401A-401D coupled to a D-type flip flop 402A-402D. Normally, the bit lines 300A-300D are maintained at a logically high level, which is passed by the comparator 401A-401D to the D-type flip flops 402A-402D as a logically low signal due to an inverted input on the comparator 401A-401D. When one of the bit lines 300A-300D is driven to a logically low level, such as by a microprocessor coupled to the corresponding **bus segment** 302A-302D, the comparator 401A-401D produces a logically high signal, which is passed to the D-type flip flops 402A-402D. Timing of the D-type flip flops 402A-402D is controlled by a conventional clock signal applied to a clock terminal (not shown) of each of the D-type flip flops 402A-402D. Thus, when a logically high signal is present on the bit lines 300A-300D, the D-type flip flops 402A-402D have a logically low signal stored therein. Alternatively, when a device attached to the bit lines 300A-300D drives a logically low signal onto the bit lines 300A-300D, a logically high signal is stored in the D-type flip flops 402A-402D.

Detail Description Paragraph - DETX (20):

[0032] The overall operation of the circuits 400A-400D may be appreciated by a description of an exemplary bus transaction. For example, assume that a logically low signal is driven onto the bit line 300B by an external device, and that none of the other **bus segments** 302A, 302C, and 302D are currently being driven by an external device. The low signal on the bit line 300B causes a logically high signal to be stored in the D-type flip flop 402B at the time that a transition occurs in the clock signal. The logically high signal is passed through the AND gate 412B to the OR gates 406A, 406C, and 406D, causing the transmitters 408A, 408C, and 408D to **repeat** or drive a logically low signal onto the bit lines 300A, 300C, and 300D, insuring that the signal initiated by the external device coupled to the **bus segment** 302B is communicated to external devices coupled to the **bus segments** 302A, 302C, and 302D. Additionally, a logically low signal is stored in the D-type flip flops 410A, 410C, and 410D,

which disables the AND gates 412A, 412C, and 412D. Thus, even though a logically low signal is being driven onto the bit lines 300A, 300C, and 300D, they are being blocked from being **repeated** on the remaining **bus segments,** as they were not initiated by the external device coupled to that **bus segment,** but rather, are being **repeated**. That is, the blockers 310A-310D prevent the **repeated** signals from being **repeated** again.

Detail Description Paragraph - DETX (21):
[0033] Those skilled in the art will appreciate that the time lag between an external device driving a signal onto its **bus segment** and the signal being **repeated** on the remaining **bus segments** corresponds to only one clock cycle. Further, standard input/output or interconnect testing of electronic devices is often accomplished using various conventional methodologies. For example, a Joint Test Access Group (JTAG) boundary scan (which is set forth in IEEE 1149.1) is commonly used. The implementation of the instant invention does not preclude the use of these standardized testing methodologies.

Claims Text - CLTX (2):
1. A method for controllably delivering signals on a bus wherein the bus is comprised of a first and second segment, the method comprising: monitoring the first **bus segment** for the presence of a first signal being driven thereon; **repeating** the first signal on the second **bus segment**; and preventing the first signal from being **repeated** on the first bus.

Claims Text - CLTX (3):
2. A method, as set forth in claim 1, further comprising: monitoring the second **bus segment** for the presence of a second signal being driven thereon; **repeating** the second signal on the first **bus segment**; and preventing the second signal from being **repeated** on the second bus.

Claims Text - CLTX (6):
5. A method, as set forth in claim 4, wherein **repeating** the first signal on the second **bus segment** further comprises driving a logically low signal on the second **bus segment**.

Claims Text - CLTX (9):
8. A method, as set forth in claim 7, wherein **repeating** the first signal on the second **bus segment** further comprises driving a logically high signal on the second **bus segment**.

Claims Text - CLTX (10):
9. A method, as set forth in claim 2, wherein monitoring the first **bus segment** for the presence of the first signal being driven thereon further comprises detecting the first signal and delivering an indication of the presence of the first signal, and wherein **repeating** the first signal on the second **bus segment** further comprises delivering the first signal on the second bus in response to receiving the indication of the presence of the first signal on the first bus.

Claims Text - CLTX (13):
12. An apparatus for controllably delivering signals on a bus wherein the bus is comprised of a first and second segment, the apparatus comprising: means for monitoring the first **bus segment** for the presence of a first signal being driven thereon; means for **repeating** the first signal on the second **bus segment**; and means for preventing the first signal from being **repeated** on the first bus.

PGPUB-DOCUMENT-NUMBER: 20020078289

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020078289 A1

TITLE: **Bus interface segments** connected by a **repeater** having two or more devices separated by a physical link

PUBLICATION-DATE: June 20, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Morrow, Neil G.	McKinney	TX	US

US-CL-CURRENT: **710/300**

ABSTRACT:

Bus **repeaters** offer electrical isolation by separating a single bus interface into one or more segments, and may provide cost advantages over bus bridges. There is a class of electrical equipment that can utilize the advantages offered by bus **repeaters,** and in addition to these advantages need to separate the **bus segments** by a distance greater than can be offered by the typical single chip **repeater**. What is disclosed here is a method for creating **bus interface segments by use of a repeater** that consists of two or more devices separated by a physical link.

---------- KWIC ---------

Abstract Paragraph - ABTX (1):

Bus **repeaters** offer electrical isolation by separating a single bus interface into one or more segments, and may provide cost advantages over bus bridges. There is a class of electrical equipment that can utilize the advantages offered by bus **repeaters,** and in addition to these advantages need to separate the **bus segments** by a distance greater than can be offered by the typical single chip **repeater**. What is disclosed here is a method for creating **bus interface segments by use of a repeater** that consists of two or more devices separated by a physical link.

Current US Classification, US Primary Class/Subclass - CCPR (1):

710/300

Title - TTL (1):

Bus interface segments connected by a **repeater** having two or more devices separated by a physical link

Summary of Invention Paragraph - BSTX (6):

[0004] Bus **repeaters** are devices that are also used to provide electrical isolation by distributing bus device loads among several **bus segments,** but require little or no configuration by a software component. Bus **repeaters** either accept and forward transactions that are not claimed by other **bus segment** devices, or are made aware by non-standard mechanisms of what address ranges to claim. A bus **repeater** may accept and forward all transactions on one

bus segment interface to the other segment. Bus **repeaters** do not create new buses in a bus hierarchy, are not typically defined by a bus interface standard, and may be used for bus interfaces that do not support a hierarchical topology.

Summary of Invention Paragraph - BSTX (10):
[0007] The present invention provides a **segment of a primary bus to be remotely located from another segment of the bus** over a physical link such as a high-speed serial bus, or any connection of electrical signals. The present invention uses a **repeater** topology rather than a hierarchical bridge topology. While bus bridges and bus **repeaters** offer similar advantages to electrical systems; their subtle functional differences greatly impact bus topology and bandwidth distribution throughout the bus topology. Bus bridges and bus **repeaters** have different configuration requirements. For example, bus **repeaters** typically have very little or no configuration required and are transparent to the system components and software.

Brief Description of Drawings Paragraph - DRTX (4):
[0014] FIG. 2 A bus **repeater** separating two **segments of a bus** with a high speed link according to an embodiment of the present invention;

Brief Description of Drawings Paragraph - DRTX (6):
[0016] FIG. 3 Another embodiment having a bus **repeater** separating two **segments of a bus** with a high speed link.

Detail Description Paragraph - DETX (3):
[0018] The present invention uses a bus **repeater** to connect two **segments of a single bus** with a physical link such as a serial bus. While the overall structure may appear somewhat similar to a bridge, the topology and functional operation within the system are different. A bus **repeater** may also used be used to provide electrical isolation by distributing bus device loads among several **bus segments or to extend a bus** to another location. But compared to a bridge, it requires little or no configuration by a software component. Bus **repeaters** either accept and forward transactions that are not claimed by other **bus segment** devices, or are made aware by non-standard mechanisms of what address ranges to claim. A bus **repeater** may accept and forward all transactions on one **bus segment** interface to the other segment. Bus **repeaters** do not create new buses in a bus hierarchy, are not typically defined by a bus interface standard, and may be used for bus interfaces that do not support a hierarchical topology.

Detail Description Paragraph - DETX (4):
[0019] With reference to FIG. 2, there is shown an embodiment of the present invention. A **repeater** 100 separates two portions of a primary **bus into segment** A 102 and segment B 104. **Repeater** 100 is separated into two half **repeater** circuits 106, 108 connected with one or more physical links 110. Thus a portion of the **repeater** is located on either side of the physical link on a separate printed circuit board and likely in a separate enclosure. The physical links are typically pairs of high speed electrical signals, a set of electrical signals dedicated to provide the physical link, or another bus such as a serial bus to enable placement of the secondary bus remotely from the primary bus. In contrast, the prior art bus bridge creates a new bus as shown in FIG. 1.

Detail Description Paragraph - DETX (5):
[0020] FIG. 3 illustrates another embodiment of the present invention. The **repeater** 200 separates bus "X" into two **bus segments** 202, 204. The **repeater**

200 consists of two half-**repeater** devices (206 and 208) separated by a physical link. These devices each consist of a **bus segment** interface block (210 and 220), and in some embodiments, decode logic for that segment (211 and 221). The decode logic determines which cycles to accept and forward to the other **bus interface segment**. A bus **repeater** may accept cycles by subtractive decode, which means no other **bus device on that segment** accepted the cycle. The decode logic may learn through subtractive decode which address ranges should be forwarded to the other segment. The decode logic for the **segment "A" bus repeater** device (11) may be different from the decode logic for the **segment "B" bus repeater** device (21).

Detail Description Paragraph - DETX (6):
[0021] When a transaction is accepted by the bus **repeater,** it is placed in a transaction queue (212 and 222) which may also contain data that corresponds to the transaction. The transaction queues may support any number of pending transactions that are destined to cross the bus **repeater**. The transaction queues for the **segment "A" bus repeater** device (212) may be different than the transaction queues for the **segment "B" bus repeater** device (222). Each bus **repeater** may implement a link translation block (213 and 223) that maps the transaction to a protocol specific to transferring the information across the physical link. If the physical link is an additional dedicated instance of the bus interface, then the translation block may not be necessary.

Detail Description Paragraph - DETX (7):
[0022] In a preferred embodiment, the **bus segments** A and B are segments of a single non-hierarchical PCI bus. The **repeater** 200 may use transaction decode as described above, or in another embodiment, the **repeater** simply **repeats** all transactions over the bus that are not claimed by any other device.

Claims Text - CLTX (2):
1. A system for extending a signal path of a host bus comprising: a first **repeater** portion connected to a first **segment of the host bus**; a second **repeater** portion connected to a second **segment of the host bus** remote from the first portion of the host bus, where the first and second portions of the **repeater** are connected by a serial link.

Claims Text - CLTX (6):
5. The system according to claim 1, wherein at least one of the **repeater** portions further comprise: an interface to the host **bus segment**; a transaction queue with a data buffer connected to the interface; a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link.

Claims Text - CLTX (7):
6. The system according to claim 3, wherein at least one of the **repeater** portions further comprise: an interface to the host **bus segment**; a transaction queue with a data buffer connected to the interface; a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link.

Claims Text - CLTX (8):
7. The system according to claim 2, wherein at least one of the **repeater** portions further comprise: an interface to the host **bus segment**; a transaction queue with a data buffer connected to the interface; a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link.

Claims Text - CLTX (12):

11. A bus **repeater** circuit comprising an interface to a host **bus segment**; a transaction queue with a data buffer connected to the interface; a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over an external serial link.

Claims Text - CLTX (13):

12. The **repeater** according to claim 9, further comprising a transaction decode circuit connected to the interface to the host **bus segment** to determine which transactions on the host bus to accept and pass on over the serial link.

US-PAT-NO: 6389501

DOCUMENT-IDENTIFIER: US 6389501 B1

TITLE: I/O peripheral device for use in a store-and-forward segment of a peripheral bus

DATE-ISSUED: May 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Garney; John I.	Portland	OR	N/A	N/A
Howard; John S.	Portland	OR	N/A	N/A
Iyer; Venkat	Portland	OR	N/A	N/A

US-CL-CURRENT: **710/310**, **710/52**

ABSTRACT:

An I/O peripheral device is equipped with a first collection of circuitry to enable the I/O peripheral device to provide a store-and-forward manner of operation to a **segment of a peripheral bus**. The first collection of circuitry includes first buffering circuitry to buffer request packets destined for a first bus agent, received from a bus controller in an integrated multi-packet form, in bulk, and at a first communication speed. Furthermore, the first collection includes control circuitry to forward the request packets separately, in a packet-by-packet basis, to the first bus agent, in a second communication speed. In one embodiment, the second communication speed is slower than the first communication speed. The I/O peripheral device further includes second buffer circuitry to buffer response packets to a request from the first bus agent provided separately, and each at the slower second communication speed. The first control circuitry also facilitates forwarding of the buffered response packets to the bus controller in bulk at the faster first communication speed. In one embodiment, the I/O peripheral device further includes second control circuitry to **repeat** communications destined for a second bus agent, received from the bus controller at the first communication speed, for the second bus agent, at also the first communication speed. In one embodiment, the I/O peripheral device is a hub.

27 Claims, 8 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

---------- KWIC ---------

Abstract Text - ABTX (1):

An I/O peripheral device is equipped with a first collection of circuitry to enable the I/O peripheral device to provide a store-and-forward manner of operation to a **segment of a peripheral bus**. The first collection of circuitry includes first buffering circuitry to buffer request packets destined for a first bus agent, received from a bus controller in an integrated multi-packet form, in bulk, and at a first communication speed. Furthermore, the first collection includes control circuitry to forward the request packets

separately, in a packet-by-packet basis, to the first bus agent, in a second communication speed. In one embodiment, the second communication speed is slower than the first communication speed. The I/O peripheral device further includes second buffer circuitry to buffer response packets to a request from the first bus agent provided separately, and each at the slower second communication speed. The first control circuitry also facilitates forwarding of the buffered response packets to the bus controller in bulk at the faster first communication speed. In one embodiment, the I/O peripheral device further includes second control circuitry to **repeat** communications destined for a second bus agent, received from the bus controller at the first communication speed, for the second bus agent, at also the first communication speed. In one embodiment, the I/O peripheral device is a hub.

Detailed Description Text - DETX (22):
Referring now to FIG. 4, wherein a block diagram illustrating a hybrid peripheral **bus having at least one segment** deployed in accordance with the store-and-forward peripheral bus of the present invention, in accordance with one embodiment, is shown. As illustrated, similar to the earlier described embodiment, hybrid peripheral bus 400 includes low speed bus agent 402 and high speed bus agent 403 coupled upstream to ports 405a and 405b of hybrid hub 404 respectively, which in turn is coupled upstream to bus controller 406. Bus controller 406 is installed on host system 410 and has associated device driver 408 that executes on host system 410. However, unlike the earlier described embodiment, hybrid hub 404 is constituted with the earlier described SF Hub 104', a conventional **repeater** type hub logic 407 and routing network 409, which selectively couples ports 405a and 405b to SF hub 104' and conventional **repeater** type hub logic 407. Conventional **repeater** type hub logic 407 is electrically equipped to operate at the faster communication speed. Thus, low speed bus agent 402 and hybrid hub 404 communicate in the lower communication speed, while hybrid hub 404 communicates with bus controller 406 and high speed bus agent 403 using the faster communication speed. In other words, in addition to not having speed shifting between transactions with other higher speed peripheral devices, to accommodate the fact that bus agent 402 operates with a slower communication speed, hybrid peripheral bus 400 actually operates with two signaling domains 432 and 434, with signaling domain 432 operating at the faster communication speed and signaling domain 434 operating at the slower communication speed.

Detailed Description Text - DETX (27):
Referring now to FIG. 4 and FIG. 6 instead, wherein in FIG. 6, a signaling protocol employed by control circuitry of SF Hub 104' to determine the communication speed capability of an attached device, in accordance with one embodiment, is shown. As illustrated, as in the prior art, upon detection of the attach pull-up, port 405a/405b drives a reset for a predetermined amount of time. Control circuitry of SF hub 104' allows the **bus segment** to settle down. After the expiration of the reset period, the control circuitry causes a predetermined signal pattern 602 to be driven through the port to the attached device, at the slower communication speed. The attached device then responds with a predetermined response pattern 604 within a predetermined time period, also at the slower communication speed. This pattern and response may **repeat** multiple times with the same or different predetermined pattern-response pairs during this exchange or negotiation period. Upon successful exchange of the requisite pattern-response pairs, for the illustrated embodiment, the control circuitry of SF hub 104' infers that the attached device is a device equipped to operate at the faster communication speed. In response, the control circuitry configures port 405a/405b to employ the parallel termination. Additionally, the control circuitry configures routing network 409 to couple port 405a/405b to **repeater** hub 407. However, if the requisite pattern-response pairs were not exchanged successfully, the control circuitry of SF hub 104' infers that the attached device is a device equipped to operate at the slower communication speed. In response, the control circuitry configures port 405a/405b to employ the serial termination instead. Furthermore, the control

circuitry configures routing network 409 to couple port 405a/405b to SF Hub 104' instead.

Current US Original Classification - CCOR (1):
710/310

Current US Cross Reference Classification - CCXR (1):
710/52

US-PAT-NO: 6192422

DOCUMENT-IDENTIFIER: US 6192422 B1
See image for Certificate of Correction

TITLE: Repeater with flow control device transmitting congestion indication data from output port buffer to associated network node upon port input buffer crossing threshold level

DATE-ISSUED: February 20, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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US-CL-CURRENT: **710/29**, 709/232 , 709/235 , **710/240** , **710/36** , **710/52** , **710/53**

ABSTRACT:

A full duplex repeater for collision-free transmission of data packets between node of a local area network. The repeater includes a multiple of ports, a signal path for communicating data between the ports, and an arbitration mechanism. Each of the ports has an input and output buffer. The mechanism routes data through the repeater by activating each of the ports one port at a time, such as with a round robin algorithm, to transmit stored data from the input buffer of an activated port through the signal path to the other ports. The repeater has a congestion control mechanism that includes level indicators and preset high and low threshold levels for the input buffers and a flow control device. The flow control device monitors the level indicators to determine if the amount of data in a buffer exceeds the high threshold level. If that occurs, the flow control device alerts the transmitting node to stop transmitting by inserting a congestion indication frame into the port's output buffer for transmission to the node. Once the amount of data in the input buffer then drops below the low threshold level, the flow control device alerts the transmitting node to resume transmitting by inserting a clear indication frame in the port's output buffer.

31 Claims, 6 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

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Brief Summary Text - BSTX (5):

Every LAN type has a set of rules, called topology rules, that dictate how the components of the network are physically connected together. Ethernet is one such set of topology rules. Background information on the Ethernet specifications and computer networks can be found in a number of references such as the IEEE 802.3 standards, Fast Ethernet (1997) by L. Quinn et al., and Computer Networks (3rd Ed. 1996) by A. Tannenbaum, which are incorporated herein by reference. Ethernet operates as a bussed network in which each of

the nodes connects to a common bus. On early Ethernet networks, all the nodes were literally attached to a single **segment of cable (the bus)** with T connectors. The network could be extended by connecting pieces of cable together with two-port **repeaters**. These **repeaters "repeat"** signals transmitted through the cable by restoring the signal's shape and strength to its original characteristics.

Current US Original Classification - CCOR (1):
710/29

Current US Cross Reference Classification - CCXR (3):
710/240

Current US Cross Reference Classification - CCXR (4):
710/36

Current US Cross Reference Classification - CCXR (5):
710/52

Current US Cross Reference Classification - CCXR (6):
710/53

US-PAT-NO: 5613077

DOCUMENT-IDENTIFIER: US 5613077 A

TITLE: Method and circuit for communication between a module and a bus controller in a wafer-scale integrated circuit system

DATE-ISSUED: March 18, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Leung; Wing Y.	Cupertino	CA	N/A	N/A
Hsu; Fu-Chieh	Saratoga	CA	N/A	N/A

US-CL-CURRENT: **710/305**, 257/E21.526 , 370/447 , 375/219 , 455/78 , **710/100** , **710/106** , 714/3

ABSTRACT:

A fault-tolerant, high-speed wafer scale system comprises a plurality of functional modules, a parallel hierarchical bus which is fault-tolerant to defects in an interconnect network, and one or more bus masters. This bus includes a plurality of **bus lines segmented** into sections and linked together by programmable bus switches and bus transceivers or **repeaters** in an interconnect network. By: 1) use of small block size (512K bit) for the memory modules; 2) use of programmable identification register to facilitate dynamic address mapping and relatively easy incorporation of global redundancy; 3) Use of a grid structure for the bus to provide global redundancy for the interconnect network; 4) Use of a relatively narrow bus consisting of 13 signal lines to keep the total area occupied by the **bus small; 5) Use of segmented bus** lines connected by programmable switches and of bus defects; 6) use of special circuit for bus transceivers and asynchronous handshakes to facilitate dynamic bus configuration; 7) use of programmable control register to facilitate run-time bus reconfiguration; 8) Use of spare bus lines to provide local redundancy for the bus; and 9) Use of spare rows and columns in the memory module to provide local redundancy, high defect tolerance in the hierarchical bus is obtained.

34 Claims, 30 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 19

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Abstract Text - ABTX (1):

A fault-tolerant, high-speed wafer scale system comprises a plurality of functional modules, a parallel hierarchical bus which is fault-tolerant to defects in an interconnect network, and one or more bus masters. This bus includes a plurality of **bus lines segmented** into sections and linked together by programmable bus switches and bus transceivers or **repeaters** in an interconnect network. By: 1) use of small block size (512K bit) for the memory modules; 2) use of programmable identification register to facilitate dynamic address mapping and relatively easy incorporation of global redundancy; 3) Use

of a grid structure for the bus to provide global redundancy for the interconnect network; 4) Use of a relatively narrow bus consisting of 13 signal lines to keep the total area occupied by the **bus small; 5) Use of segmented bus** lines connected by programmable switches and of bus defects; 6) use of special circuit for bus transceivers and asynchronous handshakes to facilitate dynamic bus configuration; 7) use of programmable control register to facilitate run-time bus reconfiguration; 8) Use of spare bus lines to provide local redundancy for the bus; and 9) Use of spare rows and columns in the memory module to provide local redundancy, high defect tolerance in the hierarchical bus is obtained.

Brief Summary Text - BSTX (16):
In accordance with the present invention, a plurality of functional modules is connected to one or more bus masters through a parallel hierarchical bus in a interconnect network. This bus includes a plurality of **bus lines segmented** into sections and linked together by programmable bus switches and bus transceivers or **repeaters** in the interconnect network.

Detailed Description Text - DETX (3):
The bus has a hierarchical structure which can be distinguished into 3 levels. As illustrated in FIG. 2, the first level or the root level has a few branches (IOB) for connecting the memory controller to the second level. In most cases, only one branch is used for the connection, unless multiple controllers are used, the other branches are used for spares. The root branches (IOB) are connected to the second level through the input-output transceivers (IOT). In the third level, the bus is arranged into quad trees with four memory modules connecting to one local bus transceiver (LT) through the local bus interconnect (LB). In the second level, the **bus is divided into bus segments** (GB) arranged into grids joined together by bus transceivers (GT) and bus switches (S). One of the bus grids is high-lighted with thicker lines in FIG. 2. The second level bus or the global bus forms the backbone of the communication network. In a system with many memory modules, loading on the global bus can be relatively heavy. To facilitate high frequency communications, bus **repeaters** or transceivers are inserted periodically to restore signal quality. By structuring the bus into a hierarchy of three levels, loading on the global bus imposed by the memory modules is decreased, in this case, by four times. In addition, loading from the global bus is shielded from the controller by the input-output transceiver (IOT). The grid structure interlaced with bus **repeaters** allows flexible bus configuration for high defect-tolerance while maintaining high-frequency bus transfers and low communication latency.

Current US Original Classification - CCOR (1):
710/305

Current US Cross Reference Classification - CCXR (5):
710/100

Current US Cross Reference Classification - CCXR (6):
710/106

US-PAT-NO: 5530813

DOCUMENT-IDENTIFIER: US 5530813 A
See image for Certificate of Correction

TITLE: Field-programmable electronic crossbar system and method for using same

DATE-ISSUED: June 25, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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US-CL-CURRENT: **710/317**, **710/100** , **710/104**

ABSTRACT:

Method and apparatus for using a field-programmable gate-array circuit as a crossbar switch. In order to connect a first port of the crossbar switch to a second port, an address within the field-programmable gate-array circuit is calculated, and a first data pattern to load at that address is determined. A second data pattern to load at that address is determined in order to disconnect the first port from the second port. The first port is then connected to the second port by loading the first data pattern at the calculated address in the field-programmable gate-array circuit. Subsequently the first port is disconnected from the second port by loading the second data pattern at the calculated address in the field-programmable gate-array circuit. Mechanisms are provided for analog or digital ports, for multiple-bit digital ports, for combinations of logical functions with the crossbar-switch functions, and for latching the data within the crossbar switch. In one embodiment, the crossbar switch is incrementally reconfigurable wherein ports not involved in the reconfiguration are not affected by the reconfiguration operation. Applications to machine vision systems are described.

63 Claims, 11 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 9

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Detailed Description Text - DETX (30):

The local busses, e.g., local bus 268, need not be programmed to extend to the entire width of the chip. In one embodiment using the AT6002 FPGA chip, the local busses are comprised of local **bus segments** which span eight (8) cells, and are then connected through a programmable **repeater** cell. The **repeater** cells can be programmed to route a signal to or from an express bus which can bypass certain sections of local bus and can thus facilitate faster signal propagation across the chip. In one embodiment, for example, each lower "East-West" local bus section is programmed to connect into any of the adjacent 8 cells (each of which cells has a left and a right "North-South" local bus associated with it), and then to connect to any of the 16 "North-South" local busses associated with those eight cells. The programmable **repeater**-cell

feature also allows routing of the signals in a zigzag manner if there is congestion in one area of the chip due, for example, to signals coming in or out from both sides of the chip on a single row or column.

Detailed Description Text - DETX (47):
In this embodiment, each cell has two Noah-South and two East-West local **bus segments** associated with it (NS1, NS2, EW1 and EW2, respectively), as shown in FIG. 4. Each local **bus segment** is eight cells long, and can be connected to the next successive local bus through programmable **repeater** cells. The **repeater** cells divide the internal cell array into sixteen zones as shown in FIG. 5. FIG. 5 is a generalized diagram of an FPGA circuit used to accommodate two bits per chip. Each **repeater** cell contains unidirectional drivers for the local busses, but the **repeater** cells can be programmed to drive the local busses in either direction.

Current US Original Classification - CCOR (1):
710/317

Current US Cross Reference Classification - CCXR (1):
710/100

Current US Cross Reference Classification - CCXR (2):
710/104

L Number	Hits	Search Text	DB	Time stamp
3	2571	segment$3 near3 (bus or busses or buses)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
4	201	(repeat$3 or retransmi$6) same (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:11
5	35	710/$.ccls. and ((repeat$3 or retransmi$6) same (segment$3 near3 (bus or busses or buses)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:10
6	0	('not' near3 (repeat$3 or retransmi$6)) same (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
7	0	('not' near5 (repeat$3 or retransmi$6)) same (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
8	0	("not" near5 (repeat$3 or retransmi$6)) same (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
9	0	("not" near5 (repeat$3 or retransmi$6)) and (segment$3 near3 (bus or busses or buses))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:19
10	0	(segment$3 near5 (bus or busses or buses)) and ("not" near5 (repeat$3 or retransmi$6))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/26 14:20